THAT WHICH IS CLAIMED IS:

1. Semiconductor memory device comprising an electrically erasable and programmable non-volatile memory cell having a single layer of gate material and including a floating-gate transistor and a control gate, characterized in that the source (S), drain (D) and channel regions of the floating-gate transistor form the control gate and in that the memory cell includes a dielectric zone (ZTN) lying between a first part (P1) of the layer of gate material and a first semiconductor active zone (RG1) electrically isolated from a second active zone (RG2) incorporating the control gate, this dielectric zone forming a tunnel zone (ZTN) for transferring, during erasure of the cell, the charges stored in the floating gate to the said first active zone.

2. Device according to Claim 1, characterized in that the capacitance of the tunnel zone (ZTN) is less than or equal to 30% of the total capacitance between the layer of gate material and all of the active zones of the memory cell.

3. Device according to Claim 1 or 2, characterized in that the transistor has an annular gate (FG) and in that the layer of gate material includes, in addition to the said annular gate (FG) and the said first part (P1), a linking part (PL) between this first part and the annular gate.

4. Device according to one of the preceding claims, characterized in that the first active zone

(RG1) and the second active zone (RG2) are electrically isolated from each other by PN junctions intended to be reverse-biased.

5. Device according to Claim 4, characterized in that the first active zone (RG1) and the second active zone (RG2) are electrically isolated from each other on the surface by an isolation region (STI).

6. Device according to Claim 5, characterized in that the first active zone (RG1) produced in a first substrate region (RG1) having a first type of conductivity, in that the second active zone is produced in a second substrate region (RG2) also having the first type of conductivity, in that the first substrate region and the second substrate region are separated by a third substrate region (RG3) having a second type of conductivity, different from the first, and in that the isolation region extends between the first substrate region and the second substrate region and includes an aperture emerging in a contact zone (PSB) in the third semiconductor region.

7. Device according to Claim 4, characterized in that the first active zone (RG1) produced in a first substrate region (RG1) having a first type of conductivity, in that the second active zone is produced in a second substrate region (RG2) also having the first type of conductivity, in that the first substrate region and the second substrate region are separated by a third substrate region (RG3) having a second type of conductivity, different from the first, and in that the layer of gate material (FG, P1,

P2) extends entirely above the three substrate regions without overlapping the isolation region (STI).

8. Device according to Claim 6 or 7, characterized in that the first substrate region (RG1) includes, on the surface, a contact zone (PC1) having the first type of conductivity.

9. Device according to Claim 8, characterized in that the first substrate region (RG1) furthermore includes a surface zone (ZS) having the second type of conductivity and extending around the said tunnel zone, this surface zone (ZS) being electrically connected to the said contact zone (PC1).

10. Device according to one of the preceding claims, characterized in that the transistor is a PMOS transistor.

11. Device according to one of the preceding claims, characterized in that it comprises a memory plane having several memory cells, each memory cell being assigned to an access transistor.

12. Device according to one of the preceding claims, characterized in that it furthermore includes bias means (MPL) possessing a memory cell programming state, a memory cell read state and a memory cell erase state, in that the bias means are capable of applying, in each of the states, predetermined voltages to the source, the drain and the substrate of the transistor and to the first active zone and in that, in the erase state, the bias means cause Fowler-Nordheim erasing by applying a voltage to the first active zone much higher

than those applied to the source, drain and substrate regions of the transistor.

13. Device according to Claim 12, characterized in that, in the erase state, the bias means (MPL) apply equal voltages to the source, drain and substrate regions of the transistor.

14. Device according to either of Claims 12 and 13, characterized in that, in the programming state, the bias means (MPL) cause hot-carrier programming within the transistor.

15. Device according to either of Claims 12 and 13, characterized in that, in the programming state, the bias means (MPL) cause Fowler-Nordheim programming by applying equal voltages to the source, drain and substrate regions of the transistor that are much higher than that applied to the first active zone.

16. Device according to one of Claims 12 to 15, characterized in that, in the read state, the drain/source voltage difference is limited to 1 volt in absolute value.

17. Device according to Claim 11, characterized in that the access transistor ($TACS_i$) assigned to a memory cell flanked by two adjacent memory cells that are located in the same column as the said memory cell in question includes a first elementary access transistor ($TACSEL1_i$) specifically associated with the said memory cell and second ($TACSEL2_i$) and third ($TACSEL3_i$) elementary access transistors respectively common to the two access

transistors assigned to the two adjacent memory cells respectively, in that the source (SLC) of the access transistor ($TACS_i$) forms the source of the first elementary access transistor while the drain of the first elementary access transistor forms part of the source of the floating-gate transistor of the memory cell and in that the device furthermore includes bias means (MPL2) capable of selecting at least one memory cell in program mode and in read mode and of erasing the memory plane by blocks of cells.

18. Device according to Claim 17, characterized in that the bias means (MPL2) are capable of applying the same source bias voltage to the respective sources of the access transistors assigned to the memory cells of any one column respectively, the same gate bias voltage to the respective gates of the access transistors assigned to the memory cells of the same column respectively and the same erase voltage to the respective first active zones of the memory cells of at least the same column.

19. Device according to Claim 17 or 18, characterized in that the access transistor ($TACS_i$) assigned to a memory cell partially surrounds the floating gate transistor of the memory cell.

20. Device according to Claim 19, characterized in that each column (CL_j) of memory cells has a layer of gate material (MTL_j) possessing a main part ($PMTL_j$) extending in the direction of the column along and opposite all the floating-gate transistors of the cells, in that the gate of the first elementary transistor of an access transistor assigned to a memory

cell includes that portion of the said main part of the layer of gate material which is located opposite the floating-gate transistor of the said cell, in that the layer of gate material includes, within each memory cell, a second, elementary portion ($E2MTL_j$) connected to the principal part and extending approximately perpendicular to this principal part on one side of the floating-gate transistor of the cell, so as to form part of the gate of the second elementary transistor of the access transistor, and a third, elementary portion ($E3MTL_j$) connected to the principal part and extending approximately perpendicular to this principal part on the other side of the floating-gate transistor of the cell, so as to form part of the gate of the third elementary transistor of the access transistor, and in that the said second elementary portion associated with a memory cell forms the third elementary portion associated with one of the two adjacent memory cells, whereas the said third elementary portion associated with the memory cell forms the second elementary portion associated with the other of the two adjacent memory cells.

21. Device according to one of Claims 17 to 20, characterized in that the bias means (MPL2) possess a programming state in which they are capable of programming a memory cell, a read state in which they are capable of reading a memory cell and an erase state in which they are capable of erasing at least one column of memory cells, in that the bias means are capable of applying, in each of the states, predetermined voltages to the sources and the gates of the access transistors, and to the drains and the substrates of the floating-gate transistors of the

cells and to the first active zones, and in that, in the erase state, the bias means cause Fowler-Nordheim erasing by applying a voltage to the first active zones that is much higher than those applied to the source regions of the access transistors, and to the drain and substrate regions of the floating-gate transistors.

22. Device according to Claim 21, characterized in that, to access a memory cell in read mode or in programming mode, the bias means (MPL2) turn on the access transistors of the memory cells belonging to the same column as that of the memory cell in question, apply an identical voltage to the source of the access transistor and the drain of the floating-gate transistor of each memory cell of the said column different from the memory cell in question and turn off the access transistors of the memory cells belonging to a column other than that of the memory cell in question.

23. Device according to Claim 14 or either of Claims 21 or 22, characterized in that the bias means (MPL; MPL2) are capable of programming a memory cell that has undergone erasure, the transistor of which cell is a PMOS transistor, by carrying out hot-electron programming on the transistor in two successive steps (PC1 = 0 V; PC1 = 5 V) so as firstly to compensate for any residual positive charges present in the floating gate and then to carry out optimum programming.

24. Device according to Claim 23, characterized in that, in the first step, the bias means (MPL1; MPL2) compensate for any residual positive

charges present in the floating gate by applying a compensation voltage (VZ1) to the contact (PC1) of the first active zone.

25. Device according to Claim 24, characterized in that the compensation voltage (VZ1) is less than or equal to 0 volts and greater than about -500 mV.

26. Device according to Claim 3 and 11, characterized in that the access transistor ($TACS_i$) assigned to a memory cell comprises a gate ($GRTACS_i$) extending perpendicular to the said linking part (PL) and on the opposite side from this linking part with respect to the annular gate, in that the source of the access transistor comprises a source contact (BL_j), in that the drain of the access transistor forms part of the source of the floating-gate transistor of the memory cell and in that the drain of the floating-gate transistor is electrically connected to the second active zone (RG2).

27. Device according to Claim 26, characterized in that all the source contacts of the access transistors of the cells of any one column of the memory plane are connected together (BL1), in that all the first active zones of the cells of any one column of the memory plane are connected together (VER1), in that the gates of the access transistors of the cells of any one line of the memory plane are connected together and the corresponding gate contacts (WLi) are connected together by a line metallization (WL1), in that the drains of the floating-gate transistors of the cells of any one line of the memory

plane are connected together in order to form another line metallization (WLP1) and in that the device furthermore includes bias means (MPL3) capable of selecting at least one memory cell in programming mode and of programming it by Fowler-Nordheim programming.

28. Device according to Claim 27, characterized in that the bias means (MPL3) are capable of selecting a cell of the memory plane and of programming it by applying a sufficient potential difference between the drain of the floating-gate transistor of the cell and the first active zone of this cell.

29. Device according to Claim 27 or 28, characterized in that the bias means (MPL3) are capable of erasing the memory plane in its entirety.

30. Device according to Claim 29, characterized in that the bias means (MP3) are capable of erasing the memory plane in its entirety by applying a high voltage to all the first active zones of all the cells and by applying a zero voltage to the other contacts of the cells.

31. Device according to one of Claims 27 to 30, characterized in that the bias means (MPL3) are capable of reading the memory plane line by line by turning on the access transistors of the cell of a line and by turning off the access transistors of the cells of the other lines.

32. Device according to one of the preceding claims, characterized in that it forms a memory of the EEPROM type or the FLASH type.

33. Integrated circuit, characterized in that it includes a device according to one of Claims 1 to 32.